**Code No: IT15213S**

**CHAITANYA BHARATHI INSTITUTE OF TECHNOLOGY (Autonomous)**

**BE (IT) II Yr I Sem (Suppl) Examination May/Jun 2015**

**DIGITAL ELECTRONICS & LOGIC DESIGN**

**Time: 3 Hours Max Marks: 75**

**Note:** Answer all questions from **Section-A** at one place in the same order

Answer any **five** questions from **Section-B**

**Section - A (25 Marks)**

1. Prove that NAND and NOR gates are universal gates (2)

2. Write a VHDL code for XOR gate (2)

3. Give the structure of PLDs (3)

4. Give the structure of FPGA (3)

5. Distinguish between synchronous and asynchronous counter with respect to speed and hardware (3)

6. What is the output signal frequency of a down counter, when fclk is the frequency of the clock (2)

7. Distinguish between Moore and Mealy type FSMs (2)

8. List and draw various symbols used in a ASM chart. Give one example. (3)

9. Define static hazard (3)

10. Define set-up and hold time of a flip-flop (2)

**Section - B (50 Marks)**

11. (a) Design a 3-input and 2-output combinational circuit. Inputs are x,y and z. The outputs

are f1 and f2. f1=∑ (0,1,4,7) and f2=∑ (2,3,4,6) (4)

(b) Write a VHDL code for the above circuit (3)

12. (a) Construct a 2:1 MUX using logic gates and construct a 4:1 MUX using 2:1 MUXes only (5)

(b) Explain the usage of “generate” statement in VHDL with a suitable example (5)

13. (a) What is edge triggering? Draw the circuit that accomplishes it and explain (5)

(b) What is a Johnson counter? How does it differ from ring counter? Explain (5)

14. (a) Explain the function of FSM as an arbiter (5)

(b) Draw the state diagram for designing a Modulo 6 counter to count the sequences 010,

111, 100, 110, 001, 101. And explain (5)

15. (a) Design an asynchronous sequential circuit to detect the sequence “111” (5)

(b) What is clock skew? Explain the significance of set up and hold time with respect to flip-flop (5)

16. (a) Write a VHDL code for a full adder circuit and explain (5)

(b) Develop a comparator circuit and explain (3)

(c) Write a VHDL code for 4-bit full adder using the full adder written for (i) (2)

17. Write detailed notes on

(a) ASM charts (5)

(b) Digital hardware design process (5)